TWINRELECT

Twinning for excellence in reliable electronics

D2.1

DELIVERABLE REPORT

D2.1 Scientific Capacity Enhancement Plan

WP2: Enhancement of Scientific Capacity

Document information

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Contents

1. Introduction

The TWIN-RELECT project unites four organizations from Europe and the UK, all focused on advancing research in the design of reliable electronics. These organizations include the University of Thessaly (UTH), the Leibniz Institute for High Performance Microelectronics (IHP) in Germany, the French National Centre for Scientific Research (CNRS), and the University of Manchester (MAN). The collaboration exemplifies a shared commitment to developing resilient and efficient electronic systems that address contemporary technological challenges. The project's primary objective is to enhance UTH's scientific and innovation capacity in the design of reliable electronic systems through strategic cooperation with the advanced partners: IHP, CNRS, and MAN.

This deliverable outlines the strategy for strengthening UTH's scientific and innovation capacity (Work Package 2). The initiative aims to develop expertise across the full spectrum of integrated circuit design, from device technology to electronic circuits and large-scale systems. This enhancement will be achieved through a structured, high-quality training program, carried out in close partnership with the collaborating institutions.

The training framework consists of four interconnected components, described in detail below, which are designed to ensure effective knowledge transfer and skill development:

1. **Joint Supervision of Early-Stage Researchers (ESRs)**: Establishing close mentorship to guide researchers in their foundational projects, fostering collaboration with field experts.
2. **Staff Exchanges**: Facilitating knowledge exchange and idea sharing through temporary placements at partner institutions.
3. **Training Schools**: Organizing specialized sessions to impart knowledge and techniques relevant to reliable integrated circuit design.
4. **Joint Experiments**: Promoting hands-on learning and collaboration by engaging participants in practical research projects.

A key focus of these activities is the involvement and development of early-stage researchers. The outcomes of the training program will not only enhance UTH’s scientific capabilities but also contribute to the academic and industrial communities through publications based on the results achieved.

The French National Centre for Scientific Research (CNRS) leads the coordination of this work package, ensuring the implementation of a coherent and impactful training program that aligns with the project’s objectives. This document serves as a guide for executing the training initiatives and achieving the work package's goals.

2. Strategy for knowledge transfer

In order to enable the organization and optimization of the proposed activities described in this document, the partners intend to **merge some of the training/exchange and evaluation events**. When compatible, they will promote activities remotely, such as webinars, online meetings, and conferences.

Streamlining Training and Exchange Events:

To enhance the efficiency of the planned activities and reduce logistical complexities, the partners propose **merging certain training and exchange events**. By combining related sessions or activities, they can minimize overlap, ensure better use of resources, and reduce travel and administrative burdens for participants. This approach allows for a more **cohesive learning experience**, where the content of multiple events can be delivered in a unified and structured manner. It also provides flexibility for participants, enabling them to engage in more concentrated learning sessions, and fosters a collaborative atmosphere across different partners.

For example, **training workshops** focused on specific technical skills or topics could be synchronized with **evaluation sessions**, such as feedback assessments or progress reports, allowing participants to review their learning outcomes immediately after engaging in the training material. Merging these events provides an opportunity for **real-time evaluation** of progress, ensuring that feedback is directly relevant to the material being covered and enabling participants to apply newly acquired knowledge immediately.

Evaluation and Progress Tracking:

The optimization strategy will also include integrated **evaluation events**, which will be strategically placed within the merged activities. This means that instead of holding separate evaluations, which can be time-consuming, participants will engage in activities that include both **learning and assessment**. For instance, hands-on workshops or collaborative projects could be followed by instant feedback and performance assessments. This integrated approach will allow for more **dynamic tracking** of individual and group progress, fostering continuous improvement and adapting the training content as needed.

Promotion of Remote Activities:

In line with the goal of increasing efficiency and reducing logistical constraints, the partners plan to leverage **remote platforms** to deliver certain activities. When feasible, activities such as **webinars, online meetings**, and **virtual conferences** will be employed to facilitate broader participation without the need for physical presence. These virtual platforms will provide the flexibility to connect with a wider audience, including partners or experts located in different regions or countries, without the costs and time commitments associated with travel.

Webinars will be used to deliver focused, expert-led sessions on specific topics, offering participants access to specialized knowledge from anywhere. These webinars can include interactive elements such as live Q&A sessions, polls, and discussions, enhancing engagement and knowledge retention.

Online meetings will serve as a platform for collaboration among team members, stakeholders, and participants. These meetings could be used for project updates, group discussions, or one-on-one consultations, making communication more efficient and accessible across time zones and locations.

Virtual conferences will bring together a larger group of participants, such as researchers, educators, or industry professionals, for a series of presentations, panel discussions, and networking opportunities. Hosting these events online will reduce the organizational complexity and make it easier for people to attend regardless of geographic location, fostering greater international collaboration and the sharing of ideas.

Enhanced Flexibility and Access:

The combination of merging events and incorporating remote activities will provide participants with greater **flexibility** in their learning and engagement. This approach ensures that participants can access high-quality content and training without the constraints of physical attendance, which can sometimes be a barrier for individuals due to cost, distance, or time limitations. Moreover, the virtual environment encourages greater **interactivity**, as participants can engage with content at their own pace, participate in discussions, and access recordings of sessions for later review.

Remote platforms will also facilitate **wider accessibility**, ensuring that more stakeholders—including those from underrepresented regions or institutions—can participate in the activities. This inclusivity promotes a broader exchange of ideas and perspectives, enriching the overall learning and collaboration process.

2.1 Work Package 2 Activities Schedule

This section provides a comprehensive timeline of activities planned in WP2, including both firm and tentative dates where applicable. Table 1 summarizes these activities, which include training schools, joint experiments, staff exchanges between partners, supervision meetings for PhD candidates, and annual project progress meetings.

Training Schools:
All training schools, one hosted by each partner, are scheduled within the first half of the project. This early timeline ensures that all partners can actively engage in scientific exchange from the start, allowing newly acquired knowledge to be integrated into the project's implementation. These schools will provide significant opportunities for early-stage researchers from UTH and partner institutions to become familiar with each other's research interests and foster collaborative relationships.

Joint Experiments:
The project includes a total of five joint experiments and one training experiment scheduled early in the project (spring 2025) in which UTH will participate as an observer. The rest of the joint experiments are distributed evenly throughout the project duration to sustain ongoing collaboration and knowledge

sharing. The dates provided in Table 1 are tentative and subject to change based on project progress and the preparation requirements of each experiment.

Staff Exchanges:
Frequent short-term visits will foster collaboration and facilitate knowledge exchange. UTH staff will visit other partners, and staff from IHP, CNRS, and UOM will visit UTH. These exchanges are scheduled to occur from Month 10 (M10) through Month 35 (M35).

PhD Supervision Meetings:
The progress of PhD candidates will be monitored through biannual supervision meetings, starting from Month 10 (M10). These meetings will ensure regular assessment and guidance, fostering the academic and professional growth of the candidates.

Annual Project Meetings:
Three annual project meetings are planned to review and evaluate the project's progress. These meetings are scheduled for July 2025, 2026 and 2027 and will take place in Volos, hosted by UTH.

Year	Month	Date	Training Schools	Joint Experiments	Visits	PHD Supervision	Annual Project Meeting
2024	0	September					
	1	October					
	2	November					
	3	December					
2025	4	January	CNRS Training School				
	5	February					
	6	March		Training Experiment, Spring 2025			
	7	April					
	8	May	IHP Training School				
	9	June				Progress Report	
	10	July	UTH Training School		Staff Exchanges		Annual Meeting
	11	August					
	12	September					
	13	October		Joint Experiment #1			
	14	November					
	15	December				Progress Report	
2026	16	January	MAN Training School				
	17	February					
	18	March		Joint Experiment #2			
	19	April					
	20	May					
	21	June				Progress Report	
	22	July		Joint Experiment #3			Annual Meeting
	23	August					
	24	September					
	25	October					
	26	November		Joint Experiment #4			
	27	December				Progress Report	
2027	28	January					
	29	February					
	30	March					
	31	April		Joint Experiment #5			
	32	May					
	33	June				Progress Report	
	34	July					Annual Meeting
	35	August					
	36	September					

Table 1: Work Package 2 Activities Indicative Schedule

3. Supervision of Early Stage Researchers (ESRs)

The supervision and professional development of Early Stage Researchers (ESRs) is a cornerstone of this project, playing a pivotal role in building their capacity for impactful research and laying the groundwork for long-term academic excellence at the University of Thessaly (UTH). To achieve these objectives, a structured and collaborative approach will be employed to guide the training, mentoring, and ongoing evaluation of the ESRs throughout the duration of the program.

At least six ESRs will be selected to join UTH's research team, with careful consideration of their alignment with the project's goals and their potential to make significant contributions to its success. The selection process will prioritize individuals with a strong foundation in their respective fields and a clear interest in the project's objectives. Each ESR will be paired with two co-supervisors: one from UTH, who will provide local mentorship and institutional guidance, and one from an advanced partner organization, who will bring specialized expertise and offer a broader, international perspective. This dual-supervision model ensures that the ESRs benefit from both a focused, local viewpoint and a wider, cross-institutional knowledge base. Together, these co-supervisors will work closely with the ESRs to define research topics, develop detailed work plans, and ensure that their research aligns with the project's thematic goals while fostering a collaborative, research-driven environment.

Training will be a key element of the ESRs' professional growth, blending theoretical learning with practical, hands-on experience. ESRs will actively participate in the activities of several Work Packages, including WP2.3, WP2.4, WP2.5, WP2.6, and WP4.4, and contribute to the research activities in WP1. This involvement will offer a wide range of opportunities for skill development, from technical expertise to practical problem-solving in real-world scenarios. The training will be delivered through a combination of on-site activities at UTH and partner institutions, as well as regular virtual meetings. These activities will serve not only as a means of knowledge transfer but also as opportunities for ESRs to engage in mentorship, share challenges, and develop solutions in a collaborative and supportive environment.

To ensure the ESRs' progress is continuously monitored and on track, their work will be assessed twice a year through formal review meetings with their co-supervisors. These meetings will be guided by progress reports submitted by the ESRs, which will outline their research milestones, the challenges they have encountered, any papers submitted or accepted, and the feedback from their supervisors. Additionally, an independent evaluation committee, composed of external experts in the scientific domain (including one or two academics), will conduct an impartial review of the ESRs' progress on an annual basis. This external evaluation, which will likely take place in conjunction with the biannual review meetings, will provide fresh insights, constructive feedback, and valuable recommendations for future directions.

Collaboration and active engagement will be a central theme throughout the entire program. Regular webinars, workshops, and online discussions will provide ESRs with consistent opportunities to present their research, seek input from peers and supervisors, and participate in academic exchanges. This interactive, dynamic approach will not only enhance their individual research efforts but also foster a strong sense of community, encouraging cross-disciplinary learning and collaboration. These platforms will also enable ESRs to stay informed about the latest developments in their fields and gain exposure to diverse perspectives.

This holistic approach to the supervision and development of ESRs is designed to equip young researchers with the skills, knowledge, and support necessary to excel in their careers. By combining personalized mentorship, rigorous training, and international collaboration, UTH aims to cultivate a new generation of researchers capable of driving innovation, making meaningful contributions to the scientific community, and shaping the future of reliable electronics. Through these efforts, the project aspires to leave a lasting impact on the academic and industrial landscape, ensuring that the next generation of researchers is well-prepared to meet the challenges of the future.

3.1 UTH PhD Students Co-supervisor Assignment

Currently, five PhD students have been identified to participate in the project, with additional candidates expected to join. Their research topics are carefully designed to align with the project's thematic goals, each covering key areas of interest. To ensure tailored guidance and access to complementary expertise, each PhD student is assigned a primary supervisor from UTH and a co-supervisor from one or two of the partner institutions (CNRS, IHP, or MAN). This assignment is summarized in Table 2 below:

UTH PhD Student	Start Date	Expected Defense Date	Topic	Local Supervisor (UTH)	Co-Supervisor (CNRS/IHP/MAN)
Nikos Chatzivangelis	Sep. 2024	2027-2028	STA, Timing Models, Process Variation, Fault Analysis	Christos Sotiriou	Luigi Dilillo (CNRS), Marko Andjelkovic (IHP)
Katerina Tsilingiri	Mar. 2024	2027-2028	Parasitic Extraction, Field Solvers, Aging, EMI	Christos Sotiriou	Fabian Luis Vargas (IHP)
Nikolaos Zazatis	Sep. 2024	2027-2028	EDA & ML, Fault Analysis	Christos Sotiriou	Davide Bertozzi (MAN), Milos Krstic (IHP)
Christos Georgakidis	Sep. 2019	May 2025	Fault Analysis, Radiation Hardening	Christos Sotiriou	Marko Andjelkovic (IHP)
Kainat Naeem	Mar. 2025 (?)	-	Parasitic Extraction, Radiation Hardening	Christos Sotiriou	TBD
TBD					

Table 2: UTH PhD Students Supervisor Assignment

The allocation of co-supervisors enables PhD students to benefit from specialized knowledge, cutting-edge resources, and a collaborative research environment. Throughout the project, supervisors will work closely with their respective students to monitor progress, provide targeted guidance, and facilitate knowledge exchange between UTH and the partner institutions. This structured approach ensures that students are well-supported in producing high-quality research outcomes that contribute to the overall success of the TWIN-RELECT project.

3.2 Abstract Descriptions of UTH Student's PhD Topics

In this subsection, a brief description of the research topics assigned to each PhD student involved in the TWIN-RELECT project is presented. These abstracts outline the key focus areas, research objectives, and expected contributions of each topic, reflecting the alignment with the project's overarching goals.

Nikos Chatzivangelis: ***Investigation of CCS Noise and OCV Models to Accurately Model and Optimize Radiation Induced SET Pulses across PVT conditions***

This PhD aims to investigate methodologies for analyzing radiation induced Single Event Transients (SETs) in Integrated Circuits (ICs), focusing on modern semiconductor technologies. As technology transistor sizes progressively shrink, digital circuits become gradually more prone to cosmic radiation, presenting significant challenges not only in aerospace but also in terrestrial applications. Existing tools and methodologies lack the scalability and precision required for industrial circuits under these conditions. This thesis will explore the use of the industrial Composite Current Source Noise (CCSN) model to develop a more accurate modelling and optimization flow for SET pulse propagation. It will also investigate integrating the model into an automated process for cell characterization, providing statistics on each gate's partial pulse (noise) immunity. Additionally, the research will examine methodologies that combine simulation and analytical approaches, including Static Timing Analysis (STA)-based methods, to enhance noise modeling accuracy for sub-20nm technologies. Another core aspect of the study involves analyzing process variation impacts and their role in radiation resilience, through On-Chip Variation (OCV) models. Furthermore, the research will consider the effects of power, voltage, and temperature (PVT) conditions on SET behaviors, aiming to develop efficient and reliable radiation analysis algorithms that account for PVT variations. Finally, the target of all the findings of this research, are to be used by an automated closed loop EDA flow for designing fault-tolerant devices. Tradeoffs between using CCSN or not for optimization of SET tolerance will be investigated and evaluated, to identify the right level of analysis. In summary, this work aims to improve current approaches by investigating a potential further increase of accuracy in fault analysis, while taking into account optimization potential, paving the way for robust circuit designs in radiation-sensitive applications.

Katerina Tsilingiri: ***Investigation of Parasitic Extraction Methods for Advanced Process Technologies***

The rapid advancement of semiconductor technology has amplified the need for accurate and efficient parasitic extraction tools to address the challenges of complex VLSI designs. The purpose of this PhD research is to develop and improve field solvers to handle challenges presented by complex geometries. The objective is to increase the scalability and computational efficiency of Field Solvers, so they can manage the complex structures of modern VLSI layouts. To achieve high precision in Parasitic Extraction for advanced circuits, the work involves optimizing for large-scale simulations, integrating advanced preconditioning techniques, and fine-tuning numerical algorithms. Moreover, this work will focus on exploring the integration of aging models into Field Solvers, with the goal of enhancing their capability to predict the impact of time-dependent degradation mechanisms, such as bias temperature instability (BTI), hot carrier injection (HCI), electromigration and dielectric breakdown, on interconnect reliability.

In this regard, not only internal IC tracks, but also lanes at the interposer level, that are used to connect different dies are of high importance. The outcomes of this research will contribute to the development of robust and reliable Field Solvers, advancing the state-of-the-art in Parasitic Extraction and enabling more accurate modeling and design of next-generation electronic systems. The correlation of this work with SETs and Fault analysis is that Parasitic Extraction Methods provide the means to generate the timing models, *e.g.* SDF file, required for STA and SET analysis.

Nikolaos Zazatis: ***Investigation of Scalable Machine Learning Methods in Electronic Design Automation***

Deep Learning has emerged as a powerful tool for addressing complex optimization problems in Electronic Design Automation (EDA). However, the computational demands and data scarcity associated with training deep models hinder their widespread adoption. This dissertation investigates Scalable Machine Learning techniques to mitigate these challenges. We propose novel approaches to reduce the computational complexity of deep models, including model quantization, pruning, and the development of dynamic neural networks. Additionally, we explore transfer learning strategies to leverage knowledge across different stages of the design flow. By combining these techniques, we aim to accelerate the design process, reduce the environmental impact of deep learning, and enable the deployment of Green AI-driven EDA tools. Furthermore, we delve into the critical issue of radiation effects, specifically Single Event Transients (SETs) and Single Event Upsets (SEUs), which can compromise the reliability of integrated circuits. We propose machine learning-based techniques to predict and mitigate the impact of these radiation-induced errors, enhancing the robustness of modern electronic systems.

Christos Georgakidis: ***Timing and SET Faults Driven Optimization Operations***

The rapid advancement of VLSI technology has revolutionised modern electrics, enabling the design and deployment of highly complex and dense integrated circuits (ICs). However, this rapid evolution has also amplified challenges associated with ensuring IC reliability, particularly in environments prone to ionising radiation. Ionising radiation can trigger transient faults known as Single Event Transients (SETs), which may propagate through digital circuits and cause functional errors, posing significant risks in safety-critical applications, such as aerospace and automotive. Traditionally, SET analysis relies on a combination of simulation-based approaches and analytical methods to evaluate the effects of these transient faults on circuit performance. While these methods are effective, they often require extensive computation or detailed technology-specific characterisation, which becomes infeasible for modern VLSI circuits comprising thousands of gates. Furthermore, with increasing circuit complexity and scaling of process nodes, there is a pressing need for efficient, scalable and technology-independent techniques to analyse and mitigate radiation-induced faults. This PhD research addresses these challenges by introducing a novel Electronic Design Automation (EDA) framework that leverages Static Timing Analysis (STA) for comprehensive SET analysis in large-scale circuits. A significant advantage of this methodology is that it performs a comprehensive SET analysis without the need for additional technology-specific characterisation, making it highly adaptable across different process technologies and design nodes.

Furthermore, it achieves a fast yet quite accurate SET analysis for circuits, allowing it to be involved in a closed-loop system design for radiation sensitivity analysis and optimisation, aiming to overall improve space digital electronics reliability, investigating the impact of several known optimisation techniques, like gate-resizing, SET filter insertion, charge-sharing etc., at this level of abstraction.

Kainat Naeem: ***Mathematical Methods for Parasitic Extraction Methods and SET Analysis***

Kainat Naeem will work on Mathematical Models for Parasitic Extraction and how to improve the state of the art of Field Solvers. Her work will cover (1) process variation modelling for metal stacks, (2) quality vs execution time tradeoffs, providing low-, medium- and high-effort solutions, with low-effort aiming to bound the timing result, (3) attempt to use spectral methods, instead of the boundary element method, if proved to be applicable and (4) incremental Extraction, solving small scale local problems when changes occur. This work will be complementary to the work by Katerina Tsilingiri, but from a foundational and theoretical perspective. The correlation to SET and Fault analysis is to provide a platform for accurate timing analysis, including metal RC parasitics.

4. Staff Exchanges

Staff exchanges form a vital component of the project, fostering collaboration and knowledge transfer between UTH and the partner institutions (IHP, CNRS, and MAN). These exchanges aim to strengthen the expertise of UTH researchers by exposing them to cutting-edge methodologies and tools employed at the partner institutions, while also enabling advanced partners to support and consolidate the training and research efforts at UTH.

The staff exchanges are organized into two key activities: short-term visits of UTH researchers to the partner institutions and short-term visits of experts from partner institutions to UTH. Together, these activities ensure a bidirectional flow of knowledge, enhancing the scientific and technical capacities of all participating teams and promoting the integration of complementary expertise. These exchanges are scheduled to commence in July 2025 (Month 10) and will continue until August 2027 (Month 35). The following subsections provide a detailed overview of these staff exchange activities, highlighting their objectives, structure, and anticipated outcomes.

4.1 Short-term visits of UTH Staff to other partners

As part of the collaborative framework of the TWIN-RELECT project, researchers from UTH will spend up to 10 months at each partner institution (IHP, CNRS, and MAN) in the form of short-term visits and structured internships. These activities aim to enhance the technical expertise of UTH researchers, promote knowledge transfer, and foster collaborative research. By participating in immersive internships, UTH researchers will gain in-depth exposure to the advanced facilities, methodologies, and research culture at the partner institutions, allowing them to acquire valuable skills directly applicable to their work within TWIN-RELECT and beyond.

4.1.1 Internships at Partner Institutions

The internships are designed to be intensive, immersive learning experiences, lasting up to three months per visit, with a primary focus on providing hands-on training. These internships will enable UTH researchers, particularly early-stage researchers, to work as embedded members of the partner institutions' research teams. This structure ensures that they not only gain exposure to advanced techniques, but also actively contribute to the research goals of both the host institution and TWIN-RELECT.

The internships will involve direct mentoring by senior researchers and domain experts at IHP, CNRS, and MAN, ensuring a tailored learning experience. Researchers will have access to the partner institutions' state-of-the-art laboratories, simulation tools, and experimental setups, allowing them to gain practical experience in cutting-edge fault-tolerant design techniques and methodologies. Additionally, UTH researchers will have the opportunity to develop transferable skills, such as the use of specialized equipment, data analysis, project management, and collaborative problem-solving.

4.1.2 Training and Activities During Visits to Partner Institutions

At IHP: Visits to IHP will focus on practical training in the characterization of faults at the circuit level and the development of fault-tolerant designs. Activities will include:

- Electrical characterization of fault effects (transient and permanent) in standard cells using SPICE simulations
- Fault injection in digital designs using commercial logic fault injector (IFSS)
- Use of AI prediction and classification methods for assessment of SET generation and propagation, and identification of critical flip-flops in the design
- Design of fault-tolerant standard cells
- Selective fault tolerance based on analytical assessment
- Design of sensors for on-chip fault detection and evaluation of the reliability of sensors
- Reconfigurable fault tolerance
- Design of test circuits and experimental setups for radiation testing
- Conducting aging, EMI and laser tests.

At CNRS: Visits to CNRS will emphasize the simulation of radiation effects and the design of experimental setups for reliability assessment. Activities will include:

- Simulating of radiation effects in scaled technologies (sub-30 nm CMOS) using in-house tool PredicSEE and ECORCE.
- Data analysis of results from in-house simulators for reliability assessment.
- Design of simulation tools for radiation effects simulations.
- Prepare test plans and test strategies for conducting tests of COTS and custom-designed chips (also furnished by project partners) in particle accelerators and TID irradiators.
- Design of hardware setups for TID, SET and SEU experiments.

At MAN: Internships at MAN will focus on fault tolerance in AI systems and neuromorphic computing. Activities will include:

- Fault tolerance analysis of AI systems.
- Simulation of spiking neural networks
- Analysis of fault effects in neuromorphic computing systems.
- Analysis of fault effects in asynchronous interconnection networks for neuromorphic computing.

4.1.3 Research, Career Advancement, and Collaboration Opportunities

In addition to the training provided to UTH staff, these visits to partner institutions pose a significant opportunity for conducting research activities. During their stay, UTH researchers will have the chance to collaborate closely with experts from the advanced partner institutions and delve deeper into specific research topics that align with both the TWIN-RELECT objectives and their ongoing PhD studies.

Under the guidance of highly qualified experts, UTH researchers can explore innovative methodologies, access state-of-the-art facilities, and leverage the specialized expertise of each institution. These interactions will not only enhance their technical and analytical skills but also foster the exchange of knowledge and ideas. This comprehensive research experience will contribute to the development of high-quality outputs, including publications in top level conferences and journals, or introduction of novel methodologies, that benefit both the individual researchers and the overall objectives of the TWIN-RELECT project.

Finally, the interactions and visits would serve as a foundation for establishing stable collaborations between UTH and the partner institutions. By actively engaging in hands-on research during their stays, UTH researchers can cultivate professional relationships and expand their academic networks, opening the way for future joint projects, co-authored publications, and other collaborative activities. This dynamic exchange will strengthen UTH's research capacity and elevate its contributions to the scientific community in alignment with the goals of the TWIN-RELECT project.

4.2 Short-term visits of IHP/CNRS/UOM staff to UTH

Besides the visits of UTH staff to partner institutions, to complement collaboration and knowledge transfer, experts from IHP, CNRS, and MAN will conduct short-term visits to the University of Thessaly (UTH). These visits are designed to strengthen joint efforts on project-related topics while providing targeted training to UTH staff. Through these interactions, the project aims to integrate the advanced expertise of partner institutions into UTH’s research initiatives, improving its scientific capacity and fostering multidisciplinary innovation.

The primary goal of these visits is to facilitate bidirectional knowledge exchange by allowing experts from partner institutions to share their specialized expertise with a wider scientific audience from UTH. By targeting early-stage researchers (ESRs) and research staff, these visits will help align UTH’s methodologies and practices with cutting-edge international research standards. Additionally, they will provide direct mentorship and co-supervision for the ESRs involved in the project, ensuring that their training and research align with both the project’s objectives and their overall research topic.

Up to six visits are planned per partner institution, with each visit lasting up to one week. During these visits, the experts will work closely with their UTH counterparts to apply and consolidate the knowledge gained during UTH’s earlier visits to the partner institutions. This synthesis of expertise will promote a unified multidisciplinary approach to research and innovation, blending the complementary strengths of the partners.

4.2.1 Training and Collaboration Activities

The visiting experts will contribute to a variety of activities during their time at UTH:

1. **Joint Research and Training**
    - Experts will actively engage in collaborative projects, assisting UTH researchers in applying the advanced methodologies and tools learned during their staying in partner institutions They will also provide hands-on guidance in integrating complementary

expertise, ensuring the smooth application of advanced techniques to ongoing research projects.

2. **Lectures and Workshops**
    - Experts will deliver lectures on scientific topics aligned with the project framework, focusing on key challenges and advancements in fault-tolerant design, reliability characterization, and related fields. These sessions will enrich the academic environment at UTH, providing ESRs and scientific staff with valuable exposure to emerging trends and state-of-the-art developments in European-level advanced research.
3. **Co-Supervision of ESRs**
    - Visiting experts will play a pivotal role in the co-supervision of ESRs, offering direct mentorship to ensure their research aligns with international standards. Face-to-face interactions will ensure a collaborative environment suited for effective mentorship, research progress and technical challenges addressing.
4. **Annual Project Progress Meeting**
    - These visits serve as an opportunity to discuss the overall progress of the project. The annual project progress meetings, held once per year in Volos, will provide a structured platform for all partners to assess the overall progress of the project. These meetings will include presentations on research activities, updates on milestones, and open discussions to address challenges and opportunities. In these sessions, all partners will attend and will actively participate, offering insights and feedback to guide the project forward.

4.2.2 Impact of IHP/CNRS/MAN Visits to UTH

These visits will significantly benefit UTH by:

- **Enhancing Research Expertise:** UTH researchers will gain advanced knowledge and technical skills, contributing to the project's success and improving their capacity for high-quality research.
- **Fostering Academic Growth:** ESRs will benefit from expert mentorship and exposure to international research practices, enhancing their professional development and career trajectories.
- **Strengthening Collaborative Ties:** The visits will deepen partnerships between UTH and the advanced institutions, laying the groundwork for sustained future collaborations, joint projects, and co-authored publications.
- **Promoting Interdisciplinary Innovation:** By integrating complementary expertise from the partners, UTH will adopt a multidisciplinary approach to address complex research challenges effectively.

The short-term visits of IHP, CNRS, and MAN staff will not only reinforce the research capabilities of UTH but also expand its scientific and academic community. They will foster a culture of innovation and excellence at UTH by enabling the direct exchange of knowledge, skills, and ideas. This initiative aligns with the fundamental goals of the TWIN-RELECT project, ensuring its long-term impact on UTH's research capacity and contributions to the broader scientific community.

5. Training Schools

To facilitate knowledge transfer and foster networking among early-stage researchers (ESRs), four dedicated training sessions, each lasting at least three days, will be organized. These sessions will serve as a platform for scientific exchange and professional development, benefiting young researchers from the University of Thessaly (UTH), partner institutions, and external participants. Each of the project partners will take responsibility for organizing one training event, ensuring diverse perspectives and expertise are brought to the program. All partners, including MAN, will actively participate in every event, further enriching the collaborative environment.

The training sessions will primarily target ESRs from UTH and partner organizations but will also welcome participation from external ESRs and research staff.

Each training session will feature:

1. **Scientific Lectures:** Focused on advanced research topics relevant to the project's scope, these lectures will be delivered by experts from partner institutions and invited speakers of international repute. They will aim to strengthen the understanding of the participants in key scientific areas and highlight innovative methodologies.
2. **Transferable Skills Training:** These sessions will cover essential professional skills such as research methodologies, scientific writing, career development, team working and communication. By equipping ESRs with these foundational skills, the training will enhance their ability to navigate interdisciplinary research environments and achieve long-term career success.
3. **Presentation of ESR Work:** Each training school will include a session dedicated to showcasing the research of early-stage researchers. This segment will provide participants with the opportunity to present their work, receive constructive feedback, and engage in meaningful discussions with other students and experts.

To complement the activities above, each training school will feature a tour of the host's facilities. This tour will provide participants with an opportunity to explore the infrastructures and ongoing research activities, while gaining valuable insight into the technologies and methodologies employed of each partner institution. This experience aims to enhance their understanding of the host's capabilities, and provide a practical perspective of real-world applications relevant to their training.

In the following subsections, the subjects of the different training schools organized by each partner are detailed.

5.1 Training School at IHP

The Training School organized by IHP will take place at the premises of IHP in Frankfurt (Oder), Germany, from 19th to 21st May, 2025. The main theme of the Training School is *Design of Reliable Integrated Circuits*.

The Training School will consist of four main events: (i) lectures given by IHP's researchers and invited external speakers, (ii) visits to IHP's clean room and laboratories, (iii) presentations of the work of PhD students (mainly from UTH), and (iv) a social event (dinner in a restaurant). The target audience are

young researchers (BSc, MSc and PhD students, and postdocs). The Training School will be open for a limited number of external participants, mainly from related projects.

The lectures at the Training School will consist of scientific and transferable skills lectures. Scientific lectures will cover all four scientific topics of the TWIN-RELECT project:

- Fault characterization and modeling
- Fault tolerance design techniques
- Reliability testing
- Methodologies for reliability analysis

The transferrable skills lectures will cover the aspects of:

- Scientific paper writing
- Preparation of project proposals
- Science marketing
- Business development

Each lecture will last 30 minutes, with additional 10 minutes for questions and discussion. All lectures given by IHP's staff will be published as open access on the TWIN-RELECT project website. If possible, the lectures given by invited speakers from external institutions will also be shared on the project website.

Since IHP is participating in two additional Twinning projects (TAICHIP and AIDA4Edge), which also address to certain extent the reliability aspects of electronic circuits and systems, a limited number of young researchers from these projects will be invited to join the Training School, thus facilitating networking and knowledge exchange between the three projects.

A minimum expected number of participants (without IHP's staff and speakers) is 30. At least 10-15 participants will be from UTH. Up to 20 participants in total will be from TAICHIP and AIDA4Edge projects and external participants (mainly from IHP's ongoing projects).

To ensure quality monitoring, a questionnaire will be prepared and distributed to all participants. The feedback from all participants will be assessed and used for possible improvement of future training events. The evaluation summary will also be presented in the respective deliverable.

5.2 Training School at CNRS

The scientific training will be focused on:

1. **Description of Natural and Artificial Radiation Harsh Environments:**
    - This section of the training will focus on understanding the different types of radiation environments that can affect electronic systems. Natural radiation comes from cosmic rays and radiation from the Earth's atmosphere, while artificial radiation sources include those from man-made environments such as nuclear reactors, space missions, or medical equipment.
    - Trainees will learn to identify the sources, behavior, and intensity of both natural and artificial radiation in various settings, and how these environments can cause degradation or failure in electronic components.
2. **Radiation-matter interaction**

- Important quantities such as stopping power, particle range and cross section will be presented
- Basic mechanisms of interaction with matter will be introduced

3. **Effect of Radiation in Terms of Single Event Effects (SEE) and Cumulative Effects such as Total Ionizing Dose (TID) and Displacement Damage (DD):**
   - **Single Event Effects (SEE):** SEE are caused by high-energy particles interacting with semiconductor devices, leading to transient faults like bit flips, latch-ups, or permanent damage. The training will cover how these effects impact the functionality of electronic systems and methods for detecting, mitigating, or designing against such events.
   - **Total Ionizing Dose (TID):** TID refers to the gradual accumulation of radiation-induced charge in a device over time, which can lead to a degradation of performance, such as a shift in threshold voltage or increased leakage currents. The training will examine how TID accumulates over the operational life of electronic systems and the techniques used to design devices that can withstand this long-term effect.
   - **Displacement Damage (DD):** DD results from the displacement of atoms in a material due to high-energy radiation, which can create defects that affect the physical properties of the material, leading to performance loss or failure. The training will explore the causes and consequences of DD on semiconductor materials and devices and how to minimize these effects during design and operation.
4. **Fault Modeling and Impact on Electronic Devices and Systems:**
   - This part of the training will address the need for fault modeling to simulate and predict the impact of radiation on electronic components and systems. Trainees will learn how to model the behavior of devices under radiation stress, including how faults such as data corruption, signal degradation, or component failure can manifest. Additionally, the training will cover strategies for analyzing and correcting faults in systems to ensure reliability and robustness in radiation-prone environments.
5. **Introduction to the simulation tool ECORCE:**
   - In this part of the training the introduction to the tool ECORCE will be done. In particular, basic topics such as the installation and license limitation will be given, as well as practical examples to simulate the interaction of ionizing particles with specific materials and topologies, which represent concrete case studies of the effect of radiation on electronics devices. These analyses enable exploring the physical phenomena and fault mechanisms at the base of device failures.
6. **Introduction to the simulation tool PREDICSEE:**
   - In this part of the training the introduction to the tool PredicSEE will be done. In particular, basic topics such as the installation and license limitation will be given, as well as practical examples to simulate the interaction of ionizing particles with specific electronic structures, such as memory cells and logic gates, which represent concrete case studies of the effect of radiation on electronics devices and retrieve fast predictive results in terms of device cross section for given radiative environments.
7. **Introduction to the access and use of irradiation facilities:**
   - This part of the training will give the basic information to new users of irradiation facilities, in order to properly operate in this content keeping the highest standard of safety for the operators and the equipment. Different scenarios will be treated depending on the type of irradiation and experiment.

Beyond the technical aspects, the training will also focus on career development, preparing trainees for real-world job opportunities in the field. The following skills will be emphasized:

1. **CV and Motivation Letter Writing:**
    - Trainees will learn how to craft an effective CV that highlights their technical and research experience in radiation effects, fault modeling, and electronic system design. They will also learn how to write a compelling motivation letter tailored to specific job applications, emphasizing their unique qualifications and passion for the field.
2. **Job Interviewing:**
    - The training will include practical advice on how to succeed in job interviews, with tips on how to present oneself confidently, answer technical questions, and demonstrate problem-solving skills. Mock interview scenarios may also be included to provide hands-on practice.

5.3 Training School at University of Manchester

The scientific training will be focused on the design of reliable deep learning systems, including those based on both artificial neural networks and spiking neural networks. Recent progress in artificial intelligence (AI) using deep learning techniques has triggered its wide-scale use across a broad range of applications. These systems can already perform tasks such as natural language processing of voice and text, visual recognition, question-answering, recommendations and decision support. However, at the current level of maturity, the use of an AI component in mission-critical or safety-critical applications can have unexpected consequences. As a result, analysing the behavior of a system under transient or permanent faults has become an essential part of the system design process. The scientific training will provide novel perspectives aiming at overcoming the traditional dichotomy between analysis at the lowest hardware design layers and system/application-level reliability analysis. Lectures and hands-on trainings will revolve around the principles and the practice of cross-layer reliability analysis.

The empirical part of the training will revolve around FLARE, a fast simulator for the cross-layer reliability analysis of deep learning accelerators specialized for the exploration of a broad architecture configuration space. The framework is composed of three major software components: (i) a C++ library containing interfaces, classes and primitives to describe hardware modules at RTL level and suitable for fast simulation through the full-cycle paradigm; (ii) a Hardware Abstraction Layer (HAL) converting the programming of hardware configuration registers into application-friendly APIs, and (iii) integration with Python for compilation as a NumPy C++ extension module. FLARE is an ongoing joint development between University of Manchester and IHP Microelectronics.

In a similar vein, spiking neural networks (SNNs) are often referred to as the third generation of neural network models. They distinguish themselves from their predecessors by their ability to mimic the actual dynamics of biological neurons more closely. In a biological brain, neurons communicate via spikes — brief, discrete events in time — which are both energy-efficient and effective for processing information due to their sparsity in time and space. Spikes are the fundamental unit of information, computation and communication in brain-inspired computers. Given their potential to revolutionize the power efficiency of many Artificial Intelligence (AI) applications, heavy research is underway on algorithms, hardware implementations, and applications of SNNs. Moving forward, in the near future the high-volume manufacturing of Integrated Circuits (ICs) and systems comprising SNNs can be foreseen, especially in

the edge computing domain where event-driven acquisition and processing pipelines hold promise of better fitting the tight power budgets of smart sensors. To this end, reliability aspects will be increasingly targeted to detect the vulnerability of SNNs to hardware issues such as silicon aging and radiation-induced soft errors. However, the radically different nature of both the neural network model and the underlying execution hardware will make reliability analysis of SNN-based neuromorphic systems a completely different problem with respect to their ANNs and accelerators counterparts. This field is still admittedly in the early stage. The scientific training will cover emerging fault models for neuromorphic systems, encompassing neuron, synapse and routing faults and their implication on SNN simulation. The empirical part of the training will put trainees in a position to start their own research in the field, by familiarizing them with state-of-the-art spiking neural network training and simulation tools and with early methodologies to link SNN simulation with hardware simulation.

The training will encompass a visit to SpiNNaker, a world-record large-scale neuromorphic computing system integrating 1 million embedded ARM cores with the capability to simulate neural networks at the level of scale of mice brains (1% of the scale of the human brain).

The transferable skills training will address the aspects of: (i) research collaboration and teamwork, (ii) narrative CV writing, (iii) interdisciplinary networking, (iv) grant writing and (v) creation and management of online profiles. Training on these skills will be given in part during the training school and in part through attendance of UTH's postdocs of the Research Staff Conference, an annual event taking place in Manchester and designed to support the career development of senior research staff through a range of workshops, panel discussions, and networking opportunities.

5.4 Training School at the University of Thessaly

The scientific training will be focused on tools and experimental techniques used in fault tolerance analysis and design:

1. **Understanding Fault Tolerance in Electronic Systems:**
    - This component of the training will provide participants with a deep understanding of **fault tolerance** — a crucial concept in the design of reliable electronic systems. Fault tolerance refers to the ability of a system to continue functioning correctly even when some of its components fail or experience faults. The training will mainly explore **hardware faults** and how to analyze and mitigate them using EDA tools.
2. **Electronic Design Automation and Fault Analysis:**
    - Participants will gain a comprehensive introduction to Electronic Design Automation (EDA), focusing on its essential role in modern circuit and system design. This section will explore the stages of the physical design flow, covering critical aspects such as design synthesis, placement, routing, and sign-off verification. It will also address challenges like power optimization, timing closure, and scalability for advanced technology nodes. Additionally, trainees will be introduced to fault analysis within the EDA workflow, learning how faults are modeled, analyzed, and mitigated using custom or commercial EDA tools. This foundation will set the stage for deeper exploration in the subsequent lectures.
3. **Techniques for Fault Tolerance Analysis:**

- This segment of the training will provide a deep dive into experimental methods for fault generation and propagation, highlighting the latest research and practical applications. In more detail, Single Event Transients (SET) and layout-based Single Event Multiple Transients (SEMT) pulse **generation models**, to simulate transient faults caused by radiation, will be presented. Additionally, **Static Timing Analysis (STA)** based methodologies for fast SET **pulse propagation** simulation will be covered as a means. These methodologies are mainly divided into two categories; the **Vector-based Dynamic Timing Analysis (DTA)** which will offer insights into fault propagation through dynamic simulations, while **Probabilistic (vector-less) SET analysis** will highlight low-overhead approaches to estimate fault behavior. Finally, the training will cover techniques for **Single Event Upsets (SEUs)**, focusing on simulation-based approaches such as SPICE or RTL simulations, as well as analytical approaches utilizing Binary Decision Diagrams (BDDs) and Algebraic Decision Diagrams (ADDs) for evaluating the reliability of combinational circuits.

4. **Techniques for Fault Tolerance Design:**
   - In addition to the fault tolerance analysis, the training will focus on practical **EDA approaches** for designing fault-tolerant Integrated Circuits. Techniques like (i) **gate resizing**, (ii) **Triple Modular Redundancy (TMR)**, (iii) **pin assignment (rewiring)**, (iv) **SET-driven placement**, and (v) **Flip-Flop spacing constraints** will be presented. This segment aims to familiarize trainees with the concept of designing fault-tolerant circuits by leveraging these techniques to enhance reliability and mitigate the effects of transient and permanent faults. Participants will explore how gate resizing can balance performance and fault tolerance, while Triple Modular Redundancy (TMR) provides robust error correction through redundancy. Pin assignment (rewiring) and SET-driven placement are introduced as effective strategies for optimizing signal routing and placement to minimize fault impact. Additionally, the application of Flip-Flop spacing constraints is discussed in the context of cell legalization, to ensure radiation-hardened designs. Together, these approaches equip participants with practical skills for implementing **fault-tolerant design solutions** in modern Integrated Circuits.
5. **Tools for Fault Tolerance Analysis:**
   - Participants will receive practical, hands-on experience with the UTH-developed SET analysis tool, *UPSET*, enabling them to apply theoretical knowledge to real-world scenarios. UPSET is a custom EDA tool following industry standards and supporting fault SPICE-like SET generation and propagation using probabilistic STA simulations. The training includes the complete tool setup process, which involves loading all the necessary files required for analysis, performing fault tolerance analysis on a selected set of designs, and extracting reliability reports. Trainees will then apply fault mitigation techniques to the designs based on the concepts presented during the training. Finally, they will extract updated reliability reports to evaluate the effectiveness of the applied mitigation techniques in reducing the overall error susceptibility of the designs. This portion of the training will teach students how to use these tools to understand system resilience and improve its robustness in radiation induced faults.

The transferable skills training will address the aspects of communication and publication strategies:

1. **Effective Communication Skills:**
    - This part of the training will focus on enhancing **communication skills** to enable participants to clearly and effectively convey complex scientific and technical information. Participants will learn how to structure and present their ideas in a way that is easily understandable to both technical and non-technical audiences. This is essential for working in interdisciplinary teams, presenting findings to stakeholders, or communicating technical concepts to a broader audience.
    - The training will also include techniques for improving **oral communication**, with a focus on **public speaking**, **presentation skills**, and **effective use of visual aids** (such as slides or data visualizations). Participants will practice delivering clear, concise, and engaging presentations that effectively communicate the importance of their work and its potential impact.
2. **Academic and Professional Writing:**
    - Participants will be trained in **scientific writing**, focusing on how to write well-structured research papers, technical reports, and project documentation. This part of the training will cover essential aspects of **scientific communication**, including proper citation practices, the use of clear and precise language, and the importance of logical flow and coherence in writing.
    - The training will provide practical guidance on writing **research papers** for publication in peer-reviewed journals, including how to structure a paper, present data, and argue scientific findings effectively.
3. **Publication Strategies:**
    - In addition to writing, the training will address strategies for getting research published. This includes an overview of the **publication process**, from selecting the right journal or conference to submitting manuscripts and responding to peer reviews. Participants will be taught how to choose an appropriate outlet for their research and how to tailor their work for different audiences (e.g., specialized academic journals vs. broader industry conferences).
    - **Open-access publishing** and the increasing importance of making research publicly available will also be covered, along with strategies for improving the visibility of published work. Participants will learn how to use platforms like **ResearchGate** or **Google Scholar** to disseminate their research and gain recognition in their field.

6. Training Trough Joint Experiments

The joint experiments outlined in this section are integral to achieving the project's objectives and strengthening collaboration among partners. These activities will leverage the ongoing participation of all beneficiaries in national and international research projects centered on fault-tolerant design. Building upon these existing efforts, the project ensures the efficient use of resources and adds significant value through shared expertise and complementary methodologies.

Each partner will contribute to the experimental activities supported by the budgets of their respective projects. The additional involvement of this project will focus on facilitating participation by covering travel and subsistence costs for team members, ensuring a broader engagement and exchange of knowledge. UTH researchers will play an active role in these experiments, gaining valuable experience and expanding their skills in experimental techniques related to the characterization of reliability.

The experimental activities are structured to cover a wide range of techniques, addressing critical aspects of fault-tolerant design. The experiments will investigate the effects of various stressors, such as radiation, accelerated aging, and electromagnetic interference (EMI), on the performance and reliability of integrated circuits. A total of five experiments are planned, alongside an initial training experiment scheduled for Spring 2025. This training experiment, conducted in collaboration with CNRS, will provide an opportunity for UTH researchers to observe advanced the preparation and execution of an irradiation experiment in practice, setting the foundation for active participation in subsequent experiments.

In the sections that follow, each experiment is described in detail, covering its objectives, methodology, and anticipated outcomes. These experiments not only contribute to the scientific and technical goals of the project but also serve to strengthen collaborative ties among the participating institutions and enhance the capabilities of early-stage researchers.

6.1 **Training experiment 1 *@CNRS/MAN/IHP*:** Ionizing particle irradiation:

In order to thoroughly analyze the impact of soft errors on the operation of selected test chips, at least one detailed experiment involving ionizing particles will be conducted. Soft errors, which are typically caused by high-energy particles, can significantly affect the functionality and reliability of integrated circuits, especially in critical applications such as space technology and high-performance computing. Understanding how these errors manifest and influence the behavior of the chips is crucial for developing fault-tolerant systems that can operate effectively under challenging conditions. To achieve this, the experiment will focus on exposing the chips to ionizing radiation, which has been identified as a key factor in causing such errors.

The specific type of ionizing particles used in the experiment will primarily depend on the availability of the necessary facilities and the requirements of the experiment. Different types of particles, such as protons, neutrons, alpha particles, or heavy ions, can be used depending on the experimental setup and the desired outcomes. The selection of particles will also be influenced by the kind of

environment that is chosen as the target for the experiment. These environments may include atmospheric conditions, where natural radiation sources like cosmic rays are present, or more controlled settings such as particle accelerators. In the case of space-related applications, particles from cosmic radiation or solar particle events will be considered, as they present significant risks to electronic systems in satellites and spacecraft.

Moreover, the experiment's design will take into account the specific radiation environments that the chips might encounter during their operational lifetime. For example, chips used in **space applications** are frequently exposed to higher levels of ionizing radiation due to the absence of the Earth's protective atmosphere. As a result, the experimental setup might include **spatial environments**, simulating the radiation exposure found in low Earth orbit or deep space. Alternatively, if a more controlled and standardized environment is preferred, **particle accelerators** could be used to precisely control the type and energy of the particles impacting the test chips.

The goal of conducting these experiments is to gather valuable data on how ionizing radiation impacts the operation and reliability of electronics, as well as to understand the failure mechanisms induced by soft errors. This data will be critical in evaluating the performance of current fault tolerance strategies and in developing new methods to enhance the resilience of electronic systems, particularly in high-risk or high-reliability applications.

6.2 **Training experiment 2 *@CNRS/IHP*:** Gamma/X-ray irradiation:

In order to thoroughly analyze the impact of Total Ionizing Dose (TID), which refers to the cumulative effect of radiation on the performance of selected test circuits, an experiment will be conducted using gamma ray (Co60) or X-ray irradiation. TID is one of the most significant radiation effects that can degrade the performance of semiconductor devices, especially in environments with high levels of ionizing radiation, such as in space or nuclear applications. Over time, exposure to radiation can accumulate in the electronic components, leading to gradual degradation in their functionality. Understanding how TID affects the circuits is crucial for designing radiation-hardened systems that can continue to operate reliably in challenging environments.

To conduct this experiment, **the PRESERVE facility**, hosted at the **IES laboratory** by the CNRS partner, will be utilized. This state-of-the-art facility is equipped to perform precise and controlled irradiation experiments, allowing researchers to simulate real-world radiation exposure in a lab setting. By using **gamma rays**, specifically **Co60** isotopes, or **X-rays**, which are both commonly used in radiation testing, the experiment will simulate the cumulative radiation dose that test circuits might encounter during their operation. **Gamma rays** from Co60 are known for their high penetration power and are typically used in radiation testing because they can accurately represent the types of radiation that components might experience in a variety of high-radiation environments. **X-rays**, on the other hand, will provide a slightly different form of radiation and can be used to study the response of the circuits to different radiation characteristics.

The experiment will focus on monitoring several critical parameters that are essential for evaluating the performance and reliability of the test circuits under radiation exposure. These include:

- **Power Consumption**: One of the primary indicators of a circuit's performance is its power consumption. Radiation-induced degradation can lead to increased leakage currents and reduced efficiency, causing a rise in the power required to operate the circuit. By monitoring power consumption, the experiment will assess how the circuits' energy efficiency is affected over time as they accumulate radiation.
- **Maximum Operating Frequency**: The maximum operating frequency of a circuit is another key performance indicator, as it determines how fast the circuit can process data or perform its intended functions. TID can cause degradation in the material properties of the semiconductor components, which can reduce the maximum operating frequency. This parameter will be carefully monitored to evaluate any shifts in the circuit's performance due to radiation exposure.
- **Transistor Voltage Threshold**: The voltage threshold of transistors is the minimum voltage required for a transistor to switch between its on and off states. Radiation exposure can cause shifts in this voltage threshold, leading to improper switching or erratic behavior in the circuit. Monitoring the transistor voltage threshold will help determine the extent to which the radiation has altered the basic operational characteristics of the transistors.
- **Functional Consistency**: Ultimately, the **functional consistency** of the circuit will be the most important aspect to monitor. This refers to the ability of the circuit to perform its intended function without errors or malfunctions, despite the exposure to radiation. Over time, radiation can cause soft errors, such as bit flips, or more severe failures in circuit logic. Functional consistency will be assessed to ensure that the circuit maintains its intended operation over the course of the radiation exposure.

By conducting this experiment, researchers aim to gather valuable data on the effects of TID on the performance and reliability of integrated circuits. The results will provide insights into how different levels of radiation exposure can affect the operation of the circuits and will help in the development of radiation-hardened technologies that can operate safely in radiation-prone environments. Moreover, this experiment will contribute to a better understanding of the long-term effects of radiation on semiconductor materials, leading to improved design methodologies for future electronic systems that need to function in challenging environments, such as in space, medical imaging, and nuclear power plants.

6.3 **Training experiment 3 *@IHP*:** Laser irradiation:

Laser fault injection is a cheap alternative to irradiation tests. Unlike irradiation tests where the whole chip is exposed to radiation, and it is difficult to identify exact particle strike locations, with laser test it is possible to precisely control the fault injection. For these purposes, a laser irradiation experiment will be conducted at IHP, utilizing an in-house setup for testing manufactured chips under laser exposure. The equipment to implement the laser fault injection consists of: a Riscure Diode Laser Station (DLS), a PC with a Riscure software for controlling the fault injection process, a stable power supply, a signal generator and an oscilloscope. The test setup is illustrated in Figure 1.

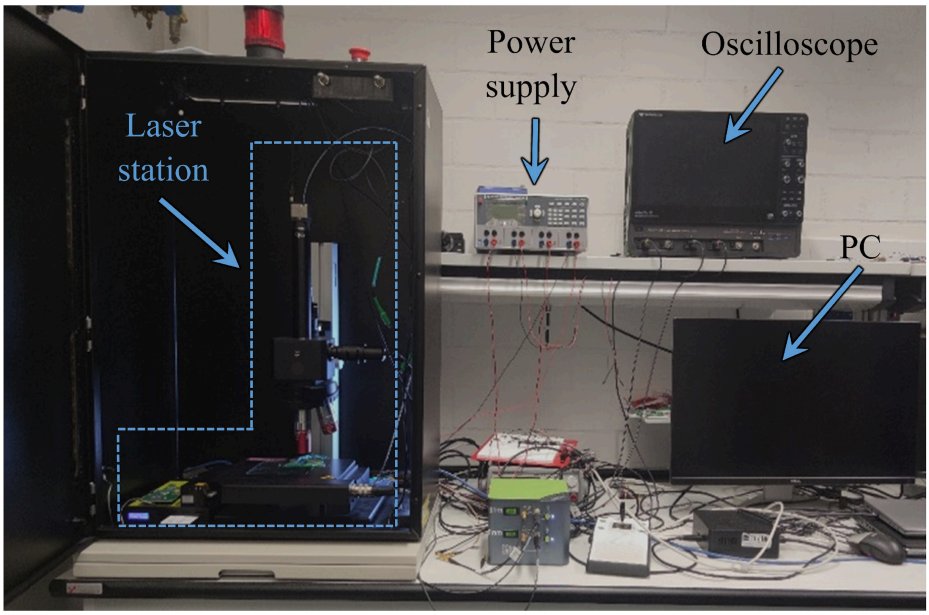

Figure 1: Laser fault injection setup at IHP

In this experiment, a variety of test chips, which have been designed using IHP's technology, will be used as test devices. These chips will specifically be chosen for their relevance to the research goals and represent a wide range of applications. The laser setup will be used to analyze and investigate the impact of soft errors on the functionality and performance of selected test chips.

Before conducting laser fault injection experiments, it is necessary to prepare the target device by removing any protective coatings or encapsulation materials that may obstruct the laser beam's path to the sensitive regions of the device. This procedure may involve decapping the device using chemical etching or mechanical techniques to expose the semiconductor die. Additionally, the effect of laser fault injection depends on various parameters, such as the laser beam wavelength, pulse duration, spot size, intensity and its distribution in a spot. Fine-tuning these parameters is crucial for effectively inducing transient faults without causing permanent damage to the target device. Two readout approaches could be applied in laser tests: (i) observing the output waveform with an oscilloscope, or (ii) observing the change of data stored in memory or sequential logic.

This advanced laser system will be carefully engineered to emulate the effects of real ionizing radiation. This will provide a controlled environment in which the behavior of electronic devices can be studied under conditions similar to those they would experience in space or other radiation-harsh environments. The test chips used for irradiation experiments may also be used for laser experiment. This allows identifying a correlation between ionizing irradiation and laser exposure.

By subjecting these chips to laser-induced radiation, the experiment will provide valuable insights into how such radiation can affect their operation, potentially leading to system malfunctions or degradation in performance. The results from this experiment are expected to contribute to the development of more resilient semiconductor devices, particularly in fields where radiation exposure is a concern, such as aerospace, nuclear, and high-energy physics applications.

6.4 **Training experiment 4 *@IHP/CNRS*:** Accelerated aging:

In order to analyze the impact of accelerated aging on integrated circuits, experiments will be performed by exposing selected chips to elevated temperature and increased supply voltage. The response of the circuit during and after the experiment will be analyzed.

During the experiment, the behavior of the integrated circuits will be continuously monitored to observe any immediate or progressive degradation in their performance. Various parameters, such as the chip's power consumption, processing speed, and error rates, will be measured to determine how the components respond to the applied stress factors. This real-time data will allow for a detailed analysis of how the circuit's functionality changes as a result of aging under these extreme conditions. Furthermore, the effects of the elevated temperature and increased voltage on the underlying material properties, such as semiconductor degradation, interconnect reliability, and thermal effects on the device, will be thoroughly examined.

After the experiment, the chips will undergo a post-experiment analysis to evaluate any lasting damage or long-term effects caused by the accelerated aging process. This phase will include a series of tests to assess whether the circuits have experienced permanent performance degradation or if they have simply been temporarily affected by the stress conditions. The results of this comprehensive analysis will provide valuable insights into the lifespan and durability of integrated circuits in high-stress environments. Moreover, these findings can contribute to improving the design and manufacturing processes of more reliable and durable chips, which are essential for critical applications, such as in aerospace, military, and automotive industries, where component failure can have serious consequences.

6.5 **Training experiment 5 *@IHP/CNRS*:** Electromagnetic Interference (EMI) for conducted and radiated noise:

One comprehensive experiment will be conducted with the objective of evaluating the impact of conducted electromagnetic interference (EMI) on the performance and reliability of selected test chips. This experiment is designed to investigate how conducting EMI, which is a form of electrical noise that moves along power lines and signal connections, can interfere with the normal operation of integrated circuits. Specifically, the conducted noise will be injected into the system through the power supply cable connected to the test board. By introducing this type of noise, the experiment aims to simulate real-world scenarios where electronic devices might be exposed to disturbances from various sources, such as nearby electrical equipment, power supply fluctuations, or other systems that emit unwanted electromagnetic radiation.

During the course of the experiment, the test chips will be subjected to varying levels of conducted EMI, and the objective is to determine the minimum intensity of this interference that is required to produce transient faults within the chip. These faults, which can cause brief disruptions or errors in the chip's operation, may lead to problems such as incorrect data processing, system malfunctions, or even temporary system failures. By gradually increasing the intensity of the conducted EMI, the

researchers will be able to identify the threshold at which these transient faults begin to occur and assess the chip's vulnerability to such disturbances.

In addition to monitoring the intensity of the conducted EMI, the experiment will also involve detailed analysis of the types of faults that occur in response to different levels of interference. This will include tracking the nature of the transient faults, such as whether they affect data integrity, timing synchronization, or overall chip functionality. The performance of the test chips will be measured continuously, with a particular focus on how the introduction of conducted EMI impacts their stability and reliability. This data will be essential for understanding the susceptibility of integrated circuits to electromagnetic noise, which is particularly important in environments where devices are expected to function in the presence of electrical interference.

Furthermore, the experiment will also consider various factors that could influence the vulnerability of the chips to conduct EMI, such as the design of the chip itself, its shielding capabilities, and the quality of the power supply system. It will be necessary to examine the response of different chip models, including variations in their architecture, to see if certain designs are more or less resilient to conducted EMI. The outcome of this experiment will provide valuable insights into the potential risks associated with conducted electromagnetic interference and will help to establish best practices for designing and testing integrated circuits that need to operate reliably in environments where EMI is a concern. These findings could have significant implications for industries that rely on the performance of electronic components in the presence of electrical noise, such as telecommunications, automotive electronics, aerospace, and medical devices.

7. Conclusions

This document has outlined a comprehensive approach for the successful implementation of the various activities designed to enhance scientific capacity, knowledge transfer, research capabilities, and professional development across the involved partners for the TWIN-RELECT EU project. Through structured activities such as **Training Schools** at key institutions like IHP, CNRS, and the University of Manchester, as well as **Joint Experimental Training** sessions, we aim to foster a collaborative environment that empowers Early Stage Researchers (ESRs) and staff with specialized skills and expertise.

The integration of **short-term visits** and **supervision programs** will further strengthen cross-institutional cooperation, ensuring that valuable experiences and insights are shared across different research environments. This cooperative approach will not only enhance the scientific and technical understanding of fault tolerance and radiation effects on integrated circuits but will also ensure the long-term sustainability of the knowledge generated through ongoing training and collaborative efforts.

The **organization methodology** outlined throughout this document ensures that all activities are executed efficiently, with clear objectives and timelines, and provides the foundation for continuous evaluation and optimization of processes. The partners are committed to achieving the goals set forth in this initiative, ensuring that all researchers and participants benefit from a robust and effective learning environment that will advance the field of fault tolerance in electronic systems and facilitate meaningful career development.